## REMARKS

After entry of the present amendments, Claims 1-3, 5-24 and 27-42 will be pending in the present application. Claims 4, 25 and 26 are cancelled herein. Claim 1 is amended to indicate that the barrier layer is a nanolaminate. Support for this amendment can be found in original Claim 4. Claim 15 has been amended to indicate that the dielectric layer and the barrier layer are deposited by an atomic layer deposition process. Support for deposition of the barrier layer by an atomic layer deposition process can be found in original Claims 25 and 26. Support for deposition of the dielectric layer by atomic layer deposition process can be found, for example, at paragraph **[0065]** of the specification. Claim 42 has been amended to indicate that the barrier layer is deposited over the dielectric layer by atomic layer deposition. Support for this amendment can be found, for example, at paragraph **[0021]** of the Specification. No new matter is added by these amendments.

Drawings

The Examiner objected to the drawings as failing to comply with 37 C.F.R. § 1.84(b)(5) because they do not include reference number "750", which is referred to in paragraph **[0054]**. Figures 21 and 22 have been amended to replace reference number "700" with "750." In addition, paragraph **[0053]** of the specification has been correspondingly amended to refer to reference number "750" rather than "700." The formal drawings are submitted herewith.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3, 5-24, 27-28, 33-38 and 40-42 were rejected under 35 U.S.C. § 102(b) as anticipated by Bai et al. (U.S. Patent No. 6,166,417). With respect to independent Claim 1, the Examiner found that Bai discloses a gate stack and an integrated circuit having a dielectric layer and a barrier layer that overlies both the PMOS and NMOS regions. Claim 1 has been amended herein to indicate that the barrier layer is a nanolaminate. There is no teaching or suggestion in Bai that the barrier layer should be a nanolaminate. As a result, Applicants request the withdrawal of the rejection of Claim 1 as anticipated by Bai. Claims 2-3 and 5-14 depend from Claim 1 and contain all of the features thereof in addition to further distinguishing features. As a result, the rejection of these dependent claims should be withdrawn as well.

With respect to Claim 15, the Examiner found that Bai discloses depositing a dielectric layer over first and second regions of a substrate, depositing a barrier layer directly over the dielectric layer, and forming first and second gate electrode layers over the first and second regions. Claim 15 has been amended herein to recite that the dielectric layer and the barrier layer are deposited by atomic layer deposition processes. Bai has no teaching or suggestion of depositing a dielectric or barrier layer by atomic layer deposition. Thus, the rejection of Claim 15 for anticipation should be withdrawn. Claims 16-24 and 27-41 depend directly or indirectly from Claim 15, and the rejection of these dependent claims should be withdrawn as well.

Similarly, independent Claim 42 has been amended to indicate that the barrier layer is deposited by atomic layer deposition. As Bai does not teach deposition of the barrier layer by atomic layer deposition, Applicants request the withdrawal of the rejection of Claim 42.

The nonobviousness of these amended claims is addressed below.

Claim Rejections Under 35 U.S.C. § 103

Claims 4, 25, and 26 were rejected under 35 U.S.C. § 103(a) as unpatentable over Bai in view of Elers et al. (WO 01/29893). The subject matter of Claim 4 has been incorporated into Claim 1 by the present amendments and Claim 4 has been cancelled. As discussed above, Bai has no teaching or suggestion of a barrier layer that is a nanolaminate. The Examiner found that Elers teaches nanolaminate barrier layers and concludes that it would have been obvious to one of ordinary skill in the art to form the barrier layer of Bai as a nanolaminate deposited by ALD because Elers teaches that a nanolaminate structure provides enhanced diffusion properties.

Applicants disagree and submit that the Examiner has failed to provide any motivation to combine the teachings of Bai and Elers. In particular, Bai has no teaching or suggestion that a nanolaminate barrier layer should be used in the disclosed transistor device. While Elers teaches nanolaminate barrier layers, the disclosure in Elers is directed to a completely different context. In Elers, the barrier layers are disclosed for use in dual damascene structures. The nanolaminate structures are deposited on low-K dielectric surfaces, etch stop surfaces and copper metal surfaces. There is no teaching or suggestion of the use of nanolaminate barrier layers in the context of metal gates.

As neither the primary reference nor the second reference has any teachings or suggestions to use a nanolaminate barrier layer in the context of metal gates, Applicants submit that the Examiner has not provided the necessary motivation to combine these references. As a

result, Applicants submit that Claim 1 is not obvious over the art of record and request withdrawal of this rejection.

Claims 25 and 26 have been cancelled. Claim 15 has been amended to recite that the dielectric layer and the barrier layer are deposited by an atomic layer deposition process. Bai has no teaching or suggestion of depositing the dielectric layer or the barrier layer by atomic layer deposition. Elers also has no teaching of a dielectric layer formed by atomic layer deposition processes. With respect to the formation of the barrier layer by atomic layer deposition, the Examiner argues that it would have been obvious to one of ordinary skill in the art to form the barrier layer by ALD because Elers teaches that a nanolaminate structure provides enhanced diffusion barrier properties and that ALD is the way in which such a structure is created.

As discussed above, Elers teaches the formation of barrier layers in the context of dual damascene structures in which high conformality is needed, thus calling for the step coverage advantage of ALD. There is no teaching or suggestion to form a nanolaminate barrier layer or any other type of barrier layer by atomic layer deposition in the context of metal gates. As a result, the Examiner has not provided any motivation to combine these references, and Applicants request withdrawal of this rejection.

Claims 29-32 were also rejected under 35 U.S.C. § 103(a) as obvious over the combination of Bai and Elers in view of Pomarede et al. (U.S. Patent No. 6,613,695). Claims 29-32 all depend from Claim 15 and include all the limitations thereof in addition to further distinguishing features. Thus, in view of the patentability of Claim 15 as discussed above, Applicants submit that the rejection of Claims 29-32 should be withdrawn as well.

Claim 39 was also rejected as obvious over Bai in view of Chang et al. (U.S. Patent No. 6,660,630). Claim 39 also depends from Claim 15 and contains all of the features thereof in addition to further distinguishing features. In view of the patentability of Claim 15, as discussed above, Applicants request withdrawal of the rejection of Claim 39 as well.

Conclusion

In view of the arguments and amendments presented above, Applicants submit that the present application is in condition for allowance and requests the same. If any issues remain, the Examiner is invited to contact Applicant's representative at the number provided below in order to resolve such issues promptly.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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